CLAIMS

What is claimed is:

1. A stackable assembly comprising:

a first carrier having a cavity therein, an upper surface, a lower surface, at least one aperture extending therethrough, and a plurality of circuits located in a portion of the cavity extending to the at least one aperture;

a semiconductor device having an active surface having a plurality of bond pads thereon, the semiconductor device located within the cavity of the first carrier;

a first connector between at least one circuit of the plurality of circuits located in the portion of the cavity of the first carrier and at least one bond pad of the plurality of bond pads on the active surface of the semiconductor device;

encapsulant material filling the portion of the cavity in the first carrier; and

connector material located in the at least one aperture in the first carrier.

2. The stackable assembly of claim 1, further comprising:

a substrate having an upper surface, a lower surface, and a plurality of circuits on the upper surface thereof; and

at least one second connector connected to the connector material in the at least one aperture in the first carrier and at least one circuit of the plurality of circuits on the upper surface of the substrate.

3. The stackable assembly of claim 1, wherein the first carrier includes at least one fin on a portion thereof.

4. The stackable assembly of claim 1, further comprising:

a second carrier oriented with respect to the first carrier and positioned the same direction as the first carrier and further having a cavity therein, an upper surface, a lower surface, at least one aperture therethrough, and a plurality of circuits located in a portion of the cavity thereon connected to the at least one aperture therethrough;

a semiconductor device having an active surface having a plurality of bond pads thereon, the semiconductor device located within the cavity of the second carrier;

a first connector between at least one circuit of the plurality of circuits located in the portion of the cavity of the second carrier and at least one bond pad of the plurality of bond pads on the active surface of the semiconductor device located in the cavity of the second carrier;

encapsulant material filling the portion of the cavity in the second carrier; and

connector material located in a second aperture in the second carrier connected to the connector material in the at least one aperture in the first carrier.

5. The stackable assembly of claim 1, wherein the first carrier includes a first frustoconical surface on a portion thereof, a second frustoconical surface on another portion thereof, and a lip on a portion of a bottom surface thereof.

6. A stackable semiconductor device assembly comprising:

a first carrier having a cavity therein, an upper surface, a lower surface, at least one aperture extending therethrough, and a plurality of circuits located in a portion of the cavity extending to the at least one aperture;

a semiconductor device having an active surface having a plurality of bond pads thereon, the semiconductor device located within the cavity of the first carrier;

a first connector between at least one circuit of the plurality of circuits located in the portion of the cavity of the first carrier and at least one bond pad of the plurality of bond pads on the active surface of the semiconductor device;

encapsulant material filling a portion of the cavity in the first carrier; and

connector material located in the at least one aperture in the first carrier.

7. The stackable semiconductor assembly of claim 6, further comprising:

a substrate having an upper surface, a lower surface, and a plurality of circuits on the upper surface thereof; and

at least one second connector connected to the connector material in the at least one aperture in the first carrier and at least one circuit of the plurality of circuits on the upper surface of the substrate.

8. The stackable semiconductor device assembly of claim 6, wherein the first carrier includes at least one fin on a portion thereof.

9. The stackable semiconductor device assembly of claim 6, further comprising:

a second carrier oriented with respect to the first carrier and positioned the same direction as the first carrier and further having a cavity therein, an upper surface, a lower surface, at least one aperture therethrough, and a plurality of circuits located in a portion of the cavity therein connected to the at least one aperture therethrough;

a semiconductor device having an active surface having a plurality of bond pads thereon, the semiconductor device located within the cavity of the second carrier;

a first connector between at least one circuit of the plurality of circuits located in the portion of the cavity of the second carrier and at least one bond pad of the plurality of bond pads on the active surface of the semiconductor device located within the cavity of the second carrier;

encapsulant material filling a portion of the cavity in the second carrier; and

connector material located in a second aperture in the second carrier connected to the connector material in the at least one aperture in the first carrier.

10. The stackable semiconductor device assembly of claim 6, wherein the first carrier includes a first frustoconical surface on a portion thereof, a second frustoconical surface on another portion thereof, and a lip on a portion of a bottom surface thereof.

11. A stackable assembly comprising:

a substrate having an upper surface, a lower surface, and a plurality of circuits on the upper surface thereof;

a first carrier having a cavity therein, an upper surface, a lower surface, at least one aperture extending therethrough, and a plurality of circuits located in a portion of the cavity extending to the at least one aperture;

a semiconductor device having an active surface having a plurality of bond pads thereon, the semiconductor device located within the cavity of the first carrier;

a first connector between at least one circuit of a plurality of circuits located in the portion of the cavity of the first carrier and at least one bond pad of the plurality of bond pads on the active surface of the semiconductor device;

encapsulant material filling the portion of the cavity in the first carrier;

connector material located in the at least one aperture in the first carrier; and

at least one second connector connected to the connector material in the at least one aperture in the first carrier and at least one circuit of the plurality of circuits on the upper surface of the substrate.

12. The stackable assembly of claim 11, wherein the first carrier includes at least one fin on a portion thereof.

13. The stackable assembly of claim 11, further comprising:

a second carrier oriented with respect to the first carrier and positioned the same direction as the first carrier and further having a cavity therein, an upper surface, a lower surface, at least one aperture therethrough, and a plurality of circuits located in a portion of the cavity therein connected to the at least one aperture therethrough;

a semiconductor device having an active surface having a plurality of bond pads thereon, the semiconductor device located within the cavity of the second carrier;

a first connector between at least one circuit of the plurality of circuits located in the portion of the cavity of the second carrier and at least one bond pad of the plurality of bond pads on the active surface of the semiconductor device located within the cavity of the second carrier;

encapsulant material filling a portion of the cavity in the second carrier; and

connector material located in a second aperture in the second carrier connected to the connector material in the at least one aperture in the first carrier.

14. The stackable assembly of claim 11, wherein the first carrier includes a first frustoconical surface on a portion thereof, a second frustoconical surface on another portion thereof, and a lip on a portion of a bottom surface thereof.

15. A stackable semiconductor device assembly comprising:

a substrate having an upper surface, a lower surface, and a plurality of first circuits on the upper surface thereof;

a first carrier having a cavity therein, an upper surface, a lower surface, at least one aperture extending therethrough, and a plurality of second circuits located in a portion of the cavity extending to the at least one aperture;

a semiconductor device having an active surface having a plurality of bond pads thereon, the semiconductor device located within the cavity of the first carrier;

a first connector between at least one second circuit of the plurality of second circuits located in the portion of the cavity of the first carrier and at least one bond pad of the plurality of bond pads on the active surface of the semiconductor device;

encapsulant material filling the portion of the cavity in the first carrier;

connector material located in the at least one aperture in the first carrier; and

at least one second connector connected to the connector material in the at least one aperture in the first carrier and at least one first circuit of the plurality of first circuits on the upper surface of the substrate.

16. The stackable semiconductor device assembly of claim 15, wherein the first carrier includes at least one fin on a portion thereof.

17. The stackable semiconductor device assembly of claim 15, further comprising:

a second carrier oriented with respect to the first carrier and positioned the same direction as the first carrier and further having a cavity therein, an upper surface, a lower surface, at least one aperture therethrough, and a plurality of circuits located in a portion of the cavity therein connected to the at least one aperture therethrough;

a semiconductor device having an active surface having a plurality of bond pads thereon, the semiconductor device located within the cavity of the second carrier;

a first connector between at least one circuit of the plurality of circuits located in the portion of the cavity of the second carrier and at least one bond pad of the plurality of bond pads on the active surface of the semiconductor device located within the cavity of the second carrier;

encapsulant material filling the portion of the cavity in the second carrier; and

connector material located in a second aperture in the second carrier connected to the connector material in the at least one aperture in the first carrier.

18. The stackable semiconductor device assembly of claim 15, wherein the first carrier includes a first frustoconical surface on a portion thereof, a second frustoconical surface on another portion thereof, and a lip on a portion of a bottom surface thereof.

19. A stackable assembly comprising:

a substrate having an upper surface, a lower surface, and a plurality of circuits on the upper surface thereof;

a first carrier having a cavity therein, an upper surface, a lower surface, at least one aperture extending therethrough, and a plurality of circuits located in a portion of the cavity extending to the at least one aperture;

a first semiconductor device having an active surface having a plurality of bond pads thereon, the first semiconductor device located within the cavity of the first carrier;

a first connector between at least one circuit of the plurality of circuits located in the portion of the cavity of the first carrier and at least one bond pad of the plurality of bond pads on the active surface of the first semiconductor device;

encapsulant material filling the portion of the cavity in the first carrier;

a first connector material located in the at least one aperture in the first carrier;

at least one second connector connected to the first connector material in the at least one aperture in the first carrier and at least one circuit of the plurality of circuits on the upper surface of the substrate;

a second carrier oriented with respect to the first carrier and positioned the same direction as the first carrier and further having a cavity therein, an upper surface, a lower surface, a plurality of connection pads on the upper surface thereof, a plurality of connection pads on the lower surface thereof, at least one first circuit of a plurality of first circuits connecting at least one connection pad of the plurality of connection pads on the upper surface thereof to at least one connection pad of the plurality of connections pads on the lower surface thereof, and at least one second circuit of a plurality of second circuits located in a portion of the cavity therein connected to the at least one connection pad of the plurality of connection pads on the upper surface thereof and the at least one connection pad of the plurality of connection pads on the lower surface;

a second semiconductor device having an active surface having a plurality of bond pads thereon, the second semiconductor device located within the cavity of the second carrier;

a third connector between the at least one second circuit of the plurality of second circuits located in the portion of the cavity of the second carrier and at least one bond pad of the plurality of bond pads on the active surface of the second semiconductor device;

encapsulant material filling the portion of the cavity in the second carrier;

at least one fourth connector connected to the at least one connection pad of the plurality of connection pads on the lower surface of the second carrier and at least one circuit of a plurality of circuits on the lower surface of the substrate.

20. The stackable assembly of claim 19, wherein the first carrier includes at least one fin on a portion thereof.

21. The stackable assembly of claim 19, further comprising:

a third carrier oriented with respect to the first carrier and positioned the same direction as the first carrier and further having a cavity therein, an upper surface, a lower surface, a plurality of connection pads on the upper surface thereof, a plurality of connection pads on the lower surface thereof, at least one first circuit of a plurality of first circuits connecting at least one connection pad of the plurality of connection pads on the upper surface thereof to at least one connection pad of the plurality of connection pads on the lower surface thereof, and at least one second circuit of a plurality of second circuits located in a portion of the cavity therein connected to the at least one connection pad of the plurality of connection pads on the upper surface thereof and the at least one connection pad of the plurality of connection pads on the lower surface thereof;

a third semiconductor device having an active surface having a plurality of bond pads thereon, the third semiconductor device located within the cavity of the third carrier;

a fifth connector between the at least one second circuit of the plurality of second circuits located in the portion of the cavity of the third carrier and at least one bond pad of the plurality of bond pads on the active surface of the third semiconductor device; and

encapsulant material filling the portion of the cavity in the third carrier.

22. A stackable semiconductor device assembly comprising:

a substrate having an upper surface, a lower surface, and a plurality of circuits on the upper surface thereof;

a first carrier having a cavity therein, an upper surface, a lower surface, at least one aperture extending therethrough, and a plurality of circuits located in a portion of the cavity extending to the at least one aperture;

a first semiconductor device having an active surface having a plurality of bond pads thereon, the first semiconductor device located within the cavity of the first carrier;

a first connector between at least one circuit of the plurality of circuits located in the portion of the cavity of the first carrier and at least one bond pad of the plurality of bond pads on the active surface of the first semiconductor device;

encapsulant material filling the portion of the cavity in the first carrier;

a first connector material located in the at least one aperture in the first carrier;

at least one second connector connected to the first connector material located in the at least one aperture in the first carrier and at least one circuit of the plurality of circuits on the upper surface of the substrate;

a second carrier oriented with respect to the first carrier and positioned the same direction as the first carrier and further having a cavity therein, an upper surface, a lower surface, a plurality of connection pads on the upper surface thereof, a plurality of connection pads on the lower surface thereof, at least one first circuit of a plurality of first circuits connecting at least one connection pad of the plurality of connection pads on the upper surface thereof to at least one connection pad of the plurality of connection pads on the lower surface thereof, and at least one second circuit of a plurality of second circuits located in a portion of the cavity therein connected to the at least one connection pad of the plurality of connection pads on the upper surface thereof and the at least one connection pad of the plurality of connection pads on the lower surface thereof;

a second semiconductor device having an active surface having a plurality of bond pads thereon, the second semiconductor device located within the cavity of the second carrier;

a third connector between the at least one second circuit of the plurality of second circuits located in the portion of the cavity of the second carrier and at least one bond pad of the plurality of bond pads on the active surface of the second semiconductor device;

encapsulant material filling the portion of the cavity in the second carrier;

at least one fourth connector connected to the at least one connection pad of the plurality of connection pads on the lower surface of the second carrier and at least one circuit of a plurality of circuits on the lower surface of the substrate.

23. The stackable semiconductor device assembly of claim 22, wherein the first carrier includes at least one fin on a portion thereof.

24. The stackable semiconductor device assembly of claim 22, further comprising:

a third carrier oriented with respect to the first carrier and positioned the same direction as the first carrier and further having a cavity therein, an upper surface, a lower surface, a plurality of connection pads on the upper surface thereof, a plurality of connection pads on the lower surface thereof, a first circuit of a plurality of first circuits connecting at least one connection pad of the plurality of connection pads on the upper surface thereof to at least one connection pad of the plurality of connection pads on the lower surface thereof, and at least one second circuit of a plurality of second circuits located in a portion of the cavity therein connected to the at least one connection pad of the plurality of connection pads on the upper surface thereof and the at least one connection pad of the plurality of connection pads on the lower surface thereof;

a third semiconductor device having an active surface having a plurality of bond pads thereon, the third semiconductor device located within the cavity of the third carrier;

a fifth connector between the at least one second circuit of the plurality of second circuits located in the portion of the cavity of the third carrier and at least one bond pad of the plurality of bond pads on the active surface of the third semiconductor device; and

encapsulant material filling the portion of the cavity in the third carrier.